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CERTIFICATE OF TRANSMISSION

November 22, 2002

Atty Docket No.:	JCLA8533
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Fax No.: 703-872-9318
Attention: Examiner MITCHELL, JAMES M
Group Unit: 2827
From: Jiawei Huang, Reg. No. 43,330
MESSAGE: Enclosed is an Amendment in 10 pages.

Sir:

I hereby certify that this correspondence is being facsimile transmitted to the Patent and Trademark Office on **November 22, 2002** at the above indicated fax number.

Sign by: Michelle Chang

Atty Docket No.: JCLA8533 **Serial No.; 10/055,568**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of: Mou-Shiung Lin, etc...	)	
	)	Examiner: Mitchell, James M
Serial No.: 10/055,568	)	Art Unit: 2827
Filed: January 22, 2002	)	Docket No.: JCLA8533
For: INTEGRATED CHIP PACKAGE STRUCTURE USING SILICON SUBSTRATE AND METHOD OF MANUFACTURING THE SAME	)	

No fee is believed to be due. However, the Commissioner is authorized to charge any fees required in connection with the filing of this paper to account No. 50-0710 (Order No. JCLA8533).

AMENDMENT AND RESPONSE TO OFFICE ACTION

BOX Non-Fee Amendment
Assistant Commissioner of Patents and Trademarks
Washington, DC 20231

Sir:

The First Office Action mailed August 28, 2002, has been carefully considered. In response thereto, please enter the following amendments and consider the following remarks.

In the Claims:

Please cancel claims 22 and 53 without prejudice or disclaimer.

Please amend claims 4 and35 as follows:

4. (Once Amended) The structure in claim 3, wherein a width, length, and thickness of traces of the external circuitry are greater than corresponding traces of the internal circuitry to reduce RC delay.

35. (Once Amended) The structure in claim 34, wherein a width, length, and thickness of traces of the external circuitry are greater than corresponding traces of the internal circuitry to reduce RC delay.

REMARKS

Present Status of the Application

The Office Action mailed August 28, 2002 rejected all presently-pending claims 1-21, 23-52, and 54-60. Specifically, claims 1-3, 5, 6-21, 25-30, 33-52, and 56-60 are rejected under 35 U.S.C. 102(b) as being anticipated by Akagawa, U.S. Patent No. 6,121,688; claims 1, 22, 23, 30-32, 53, and 54 are rejected under 35 U.S.C. 102(b) as being anticipated by Shanefield, U.S. Patent No. 4,866,501; and claim 4 and 35 are rejected under 35 U.S.C.103(a) as being unpatentable over Akagawa, U.S. Patent No. 6,121,688. The Applicants have amended claims 4 and 35 to clearly define the limitations and features and cancelled claims 22 and 53 without disclaimer or prejudice.

After entry of the foregoing amendments, claims 1-21, 23-52, and 54-60 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Summary of Applicant's Invention

The present invention presents a chip package structure and method of manufacturing the same by adhering the backside of a die to a silicon substrate, wherein the active surface of the die has a plurality of metal pads. A thin-film circuit layer is formed on top of the die and the silicon

substrate, where the thin-film circuit layer has an external circuitry that is electrically connected to the metal pads of the die. The external circuitry extends to a region that is outside the active area of the dies and has a plurality of bonding pads located on the surface layer of the thin-film layer circuit. The active surface of the die has an internal circuitry and a plurality of active devices, where signals can be transmitted from one active device to the external circuitry via the internal circuitry, then from the external circuitry back to another active device via the internal circuitry. Furthermore, the silicon substrate has at least one inwardly protruded area so the backside of the die can be adhered inside the inwardly protruded area and exposing the active surface of the die. Wherein the silicon substrate is composed of a silicon layer and a heat insulating material formed overlapping and the inwardly protruded areas are formed by overlapping the silicon substrate with openings on the heat conducting layer. Futhermore, the present chip package structure allows multiple dies with same or different functions to be packaged into one integrated chip package and permits electrically connection between the dies by the external circuitry.

Discussion of Office Action Rejections under 35 U.S.C. 102(b) over Akagawa

A preliminary discussion of the differences between the technology and structure disclosed in Akagawa and the present invention is appropriate. In this regard, there is a fundamental

difference in the structure and technique. Akagawa is directed to an exclusive use of his anisotropic conductive sheet in a circuit board which can reduce the thickness and complexity of the circuit board which teaches away from the present invention.

A special anisotropic conductive sheet is disposed between the chip and the above layers which replaces conventional pair of conductive and dielectric layers. A special anisotropic conductive sheet comprising a resin and conductive fillers, such as metallic particles, added in the resin is heat-pressed at the point where conductivity is required because the pressure and heat will force the metallic particles to allow conductivity in the vertical direction. The anisotropic layer is processed during the formation which is similar to a conventional flip chip process for connecting the active surface of the chip to an external connector. Akagawa only teaches a post-process on which does is different from the IC+substrate process of the present invention.

In contrast, the present invention provides an integrated chip package structure using silicon substrate to provide redistribution of bonding points with reduced thickness and increased life span and durability. The redistribution of the bonding points on a die is achieved by the use of a thin-film circuit layer which allows the bonding points to extend laterally outside the original active surface area of the die to meet standard pitch requirement. The present invention processes both the IC and the substrate to achieve its objects.

Akagawa solves an entirely different problem regarding production cost and thickness of the resultant product and does not disclose any information regarding redistribution of bonding points to meet standard pitch requirement and the use of thin-film circuit layer. It is to be noted that the anisotropic conductive layer with metallic fillings is inherently different from the thin-film circuit layer of the present invention because anisotropic layer requires heat pressing of the anisotropic conductive layer to allow conductivity. Akagawa is clearly teaching away from the present invention by taking a path different from the present invention by using anisotropic conductive layer, in which a person skilled in the art would be diverged by the path set forth by Akagawa.

Akagawa teaches a multi-chip module in FIG. 6 with two chips and a common substrate. Akagawa only discloses the method of connecting an external connector to the metal pads of the chip but does not disclose any information regarding the redistribution of the bonding points. Akagawa does not teach any post-processing on the substrate after its formed. Akagawa addresses all the issues regarding connections with the special anisotropic conductive film because it provides flexibility in forming the connectors. Furthermore Akagawa does not disclose the cited feature of claim 1 and 30 of the present invention, which is that "the external circuitry extends to a region outside the active surface of the die..., the external circuitry has a

plurality of bonding points... electrically connected to corresponding metal pads of the die", as clearly illustrated in FIG. 1I *(emphasis added)*. It can be seen in FIG. 1I of the present invention that the bonding pads are clearly outside the active surface of the chip. Therefore Akagawa fails to anticipate the claimed feature of present invention and cannot be used to render claims 1-3, 5, 6-21, 25-30, 33-52, and 56-60 rejected. Withdrawal of the rejections of these claims is sincerely requested.

Discussion of Office Action Rejections under 35 U.S.C. 102(b) over Shanefield

A preliminary discussion of the differences between the technology and structure disclosed in Shanefield and the present invention is appropriate. In this regard, there is a fundamental difference in the structure and technique. Shanefield is directed to wafer scale integration by having a depression or a hole to hold a chip in it. As a result, the package is higher in density and speed. Shanefield only discloses a method of encapsulating a chip within a substrate so the surface of the chip lies essentially in the same plane as the surface of the wafer.

Shanefield teaches a conductive foil applied by tape automated bonding (TAB) as the connection between the chip and the bonding pads. Shanefield does not disclose any information regarding the redistribution of the bonding points of a chip and furthermore the claimed feature as cited in claim 1 which reads "a thin-film circuit layer located on top of the

silicon substrate and the die and has an external circuitry, wherein the external circuitry is electrically connected to the metal pads of the die and extends to a region outside the active surface of the die"*(emphasis added)*. Shanefield teaches a chip structure that does not involve any post-processing on the chip or the substrate. Shanefield also fails to disclose an integrated substrate by combining a silicon layer and a heat conducting layer. Although Shanefield discloses the use of an additional heat sink which forms beneath the main substrate as the support/heat-sink layer, it is substantially and patentablely different from the integrated substrate by combining silicon blocks to a heat conducting layer to form the holes. Furthermore Shanefield only teaches post-process on the substrate and is different from the IC+substrate process of the present invention. Furthermore Shanefield does not disclose the cited feature of claim 1 and 30 of the present invention, which is that "the external circuitry extends to a region outside the active surface of the die..., the external circuitry has a plurality of bonding points... electrically connected to corresponding metal pads of the die", as clearly illustrated in FIG. 1I *(emphasis added)* As a result, Shanefield fails to anticipate the claimed feature of the present invention and therefore cannot be used to render claim 1, 23, 30-32, and 54 rejected. Withdrawal of the rejections of these claims is sincerely requested.

Discussion of Office Action Rejections under 35 U.S.C. 103(a) over Akagawa

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The Office Action states that "it would have been an obvious matter of design choice" for claims 4 and 35. The Applicants respectfully disagree because Akagawa does not teach the anisotropic conductive layer, which is known equivalent to the thin-film circuit of the present invention by the Examiner, to have wider, thicker, and longer traces to alleviate RC delay. Akagawa does not disclose any information on the width, thickness, and length of the circuit pattern on the anisotropic layer. However the Applicants have amended claim 4 and 35 to clearly indicate the unobvious reason for such dimensional characteristics.

CONCLUSION

For at least the foregoing reasons, it is believed that all pending claims 1-21, 23-52, and 54-60 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
J.C. PATENTS

Date: 11/22/2002

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